

IN THE CLAIMS

1. (Original) A method for processing images, implementing a calculation of cumulative histogram values based on N histogram values, said method being characterized in that it comprises calculation stages which use at least two parallel additions, each addition in a calculation stage leading to an addition result based on two histogram values or one histogram value and one addition result calculated during a previous calculation stage or two addition results calculated during at least one previous calculation stage.
2. (Original) A method for processing images as claimed in claim 1, characterized in that the calculation method comprises at least two successive series of calculation stages, each series of calculation stages being intended to calculate cumulative histogram values that correspond to a group of histogram values that includes a number of histogram values that is strictly lower than N.
3. (Original) A calculation circuit for calculating cumulative histogram values based on histogram values, said circuit comprising at least two adders able to perform additions in parallel during calculation stages, each addition during a calculation stage leading to an addition result based on two histogram values or one histogram value and on an addition result calculated during a preceding calculation stage or two addition results calculated during at least one preceding calculation stage.
4. (Original) An image processing system comprising a calculation circuit as claimed in claim 3.
5. (Original) A Set Top Box comprising at least an image processing system as claimed in claim 4.
6. (Original) A device comprising at least a screen intended to display images and an image processing system as claimed in claim 4.

7. (Original) A communication network comprising at least a transmitter able to send signals representing at least one image, a transmission network, a receiver able to receive said signals and an image processing system as claimed in claim 4.

8. (Currently amended) A program comprising program code instructions for the execution of the stages of the method as claimed in ~~one of the claims 1 or 2~~claim 1 if said program is executed on a processor.